DELAYED-LOCKED LOOP WITH FINE AND COARSE CONTROL USING CASCADED PHASE INTERPOLATOR AND VARIABLE DELAY CIRCUIT

ABSTRACT OF THE DISCLOSURE

A delay-locked loop (DLL) circuit includes a phase interpolator circuit and variable delay circuit coupled in cascade and operative to generate an output clock signal that is delayed with respect to a reference clock signal responsive to respective first and second control signals applied to the phase interpolator and the variable delay circuit. The DLL circuit further includes a phase control circuit that generates the first and second control signals responsive to the output clock signal and the reference clock signal. The variable delay circuit may provide a coarser resolution than the phase interpolator circuit, for example, the variable delay circuit may include a tapped delay chain circuit configured to provide step changes in delay responsive to the second control signal. The phase control circuit may be operative to cause the phase interpolator circuit to shift from one extreme of a delay range thereof towards another extreme of the delay range concurrent with a step change in delay through the variable delay circuit to thereby limit overcompensation.